

## REMARKS

The present application was filed on December 24, 2001 with claims 1-21. Claims 1, 7, 12, 16 and 19 are the independent claims.

In the outstanding Office Action, the Examiner: (i) rejected claim 15 under 35 U.S.C. §112, second paragraph; (ii) rejected claims 1, 5, 7, 10, 12, 15, 16 and 19 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,330,684 to Yamanaka et al. (hereinafter "Yamanaka"); and (iii) rejected claims 2-4, 6, 8, 9, 11, 13, 14, 17, 18, 20 and 21 under 35 U.S.C. §103(a) as being unpatentable over Yamanaka.

In this response, Applicants respectfully traverse the various §112, §102(e), and §103(a) rejections for at least the following reasons.

With regard to the issue of whether claim 15 is indefinite in accordance with §112, second paragraph, Applicants assert that such is not the case. Claim 15 recites that in the Viterbi decoder of claim 12, the add-compare-select algorithm is implemented in accordance with an integrated circuit device. Applicants believe that such claim is not indefinite in any way. By way of example only, it is known that integrated circuits such as digital signal processors (DSPs) can be programmed to implement steps of an algorithm. Further, integrated circuits can be designed and configured to implement steps of an algorithm. Accordingly, Applicants believe that claim 15 is definite.

With regard to the issue of whether claims 1, 5, 7, 10, 12, 15, 16 and 19 are anticipated under 35 U.S.C. §102(e) by Yamanaka, the Office Action contends that Yamanaka discloses all of the claim limitations recited in the subject claims. Applicants respectfully assert that Yamanaka fails to teach or suggest all of the limitations in claims 1, 5, 7, 10, 12, 15, 16 and 19, for at least the reasons presented below.

It is well-established law that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Applicants assert that the rejection based on Yamanaka does not meet this basic legal requirement, as will be explained below.

The present invention, for example, as recited in independent claim 1, recites a method of performing add-compare-select operations in accordance with a Viterbi decoder comprising the following steps. Input values of two or more sets of input values are respectively added to generate

sums for the two or more sets. Substantially concurrent with the respective addition of the input values of the two or more sets of input values, the two or more sets of input values are compared. One of the generated sums of the two or more input sets is selected based on the comparison of the two or more sets of input values. Independent claims 7, 12, 16 and 19 recite similar limitations.

The Office Action cites FIG. 6 of Yamanaka in support of the rejection of independent claims 1, 7, 12, 16 and 19. The add and compare operations performed by the ACS processing unit of FIG. 6 of Yamanaka are described in columns 5 through 7. With regard to comparing section 5, adding section 6, and selecting section 8, Yamanaka states:

First, two path metrics (PM1, PM0) are output to the bus 2 from the path metric storing section 1. On the other hand, two branch metrics (BM1, BM0) are output to the bus 4 from the branch metric storing section 3.

The comparing section 5 inputs two path metrics (PM1, PM0) from the bus 2 and two branch metrics (BM1, BM0) from the bus 4 so as to calculate  $PM1+BM1-PM0-BM0$ .

The adding section 6 inputs two path metrics (PM1, PM0) from the bus 2 and two branch metrics (BM1, BM0) from the bus 4 so as to calculate  $PM1+BM1$  and  $PM0+BM0$ . Then, the calculation results (as  $PM1+BM1$ ,  $PM0+BM0$ ) are output to the selecting section 8.

The selecting section 8 inputs the most significant bit (hereinafter referred to as "MSB") which is the code bit of the comparison result of the comparing section 5,  $PM1+BM1-PM0-BM0$ . Then, the selecting section 8 selects as to whether the high order  $PM1+BM1$  is output to the bus 13 or the low order  $PM0+BM0$  is output thereto from the value of the MSB.

However, despite the contention in the Office Action to the contrary, no where does this portion of Yamanaka, nor any other portion of Yamanaka, disclose that “substantially concurrent with the respective addition of the input values of the two or more sets of input values, the two or more sets of input values are compared,” as recited in the claimed invention. The fact that a block diagram (FIG. 6 of Yamanaka) illustratively depicts a “comparing section” next to an “adding section” does not give rise to a conclusion that Yamanaka discloses that “substantially concurrent with the respective addition of the input values of the two or more sets of input values, the two or more sets of input values are compared,” as recited in the claimed invention.

Column 6, lines 7-11, of Yamanaka state that “two path metrics could be updated

simultaneously by processing the ACS operation in parallel.” However, as is made clear by FIG. 6, Yamanaka is referring to parallelism between two separate ACS operations, not substantial concurrence between add and compare operations.

With regard to the issue of whether claims 2-4, 6, 8, 9, 11, 13, 14, 17, 18, 20 and 21 are unpatentable under 35 U.S.C. §103(a) based on Yamanaka, the Office Action contends that while Yamanaka may fail to disclose the various claim limitations recited in the subject claims, it would have been obvious to one ordinarily skilled in the art to modify Yamanaka to yield the claimed invention. Applicants respectfully assert that Yamanaka fails to disclose the proper motivation to be modified to yield the claimed invention.

While Applicants assert that claims 2-4, 6, 8, 9, 11, 13, 14, 17, 18, 20 and 21 are patentable over Yamanaka in view of the remarks above with respect to the independent claims from which they depend, it is also asserted that such claims recite patentable subject matter in their own right.

By way of example, claim 3 recites wherein the comparison operation further comprises performing carry save addition on the two sets of input values, and evaluating a carry output of the carry save addition operation to make the determination as to which set of the two or more sets would result in the largest sum. Claims 9, 14, 18 and 21 recite similar limitations. No where does Yamanaka disclose or even suggest motivation to be modified to provide a comparison operation that comprises performing carry save addition.

As illustratively explained in the present specification at page 5, lines 14-22:

Carry save addition: This is an approach used for the evaluation of multi-operand addition. A prime example is partial product summation in multipliers. In carry save addition, the time consuming carry propagations are not performed. Rather, the carries generated at various bit positions are saved as another binary number. For example, in a three operand addition involving a single level of full adders, two outputs from the full adder network, i.e., sum and carry, together represent the result. In order to form the final result as a single binary number, these binary numbers (sum and carry) should be added together (carry propagate addition). In contrast to carry propagate addition, carry save addition always produces results in sum and carry form, wherein each of the sum and carry are binary numbers themselves.

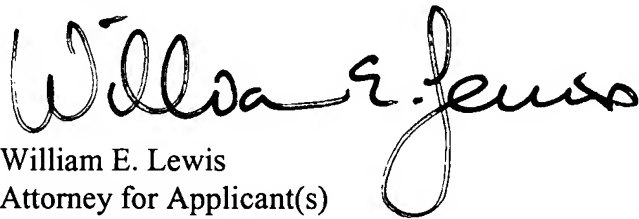
While column 13, lines 25-31, of Yamanaka mentions a carry input of comparator 26, no where does Yamanaka disclose or even suggest motivation to be modified to provide a comparison operation that comprises performing carry save addition, as recited in claim 3.

Furthermore, while Yamanaka mentions 4:2 compressors, no where does Yamanaka disclose or even suggest motivation to be modified to provide a comparison operation wherein the carry save addition operation is performed by one or more data compressors, as recited in claim 4. The 4:2 compressor in Yamanaka appears to be used in the addition operation, not the comparison operation.

Still further, no where does Yamanaka disclose or even suggest motivation to be modified to provide a comparison operation that begins when the input values of the two or more sets are available such that the comparison operation is completed before completion of the addition operation, as recited in claims 6 and 11. The rationale in the Office Action referring to engineering design choice is merely conclusory and fails to provide any reasoning for how a reference such as Yamanaka, which does not disclose substantially concurrent add and compare operations, can be modified to provide a comparison operation that begins when the input values of the two or more sets are available such that the comparison operation is completed before completion of the addition operation, as recited in claims 6 and 11.

In view of the above, Applicants believe that claims 1-21 are in condition for allowance, and respectfully request withdrawal of the various §112, §102(e), and §103(a) rejections.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "William E. Lewis". The signature is fluid and cursive, with the first name "William" being the most prominent part.

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